Extreme Environment Interconnects and Packaging for Power Electronics

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Abstract—This paper presents the combination of an innovative assembly and packaging process utilising Solid Liquid Inter Diffusion (SLID) Cu-Sn interconnects within bespoke ceramic substrates that have been produced using Additive Manufacturing (AM). The resultant process chain supports the integration and packaging of power electronics for harsh environment applications. In this work, we investigate how the bond strength and mechanical integrity of Cu-Sn SLID interconnects are affected after being exposed concurrently to vibration and thermal loading ("shake and bake test") . Test vehicles were exposed simultaneously to thermal loading up to 300 °C and mechanical loading in terms of high random frequency vibration between 1 Hz and 2000 Hz, which is closely associated with the aerospace and oil & gas industries maximum operating conditions. In parallel micro-extrusion printing methods in which high viscosity ceramic pastes are dispensed through cylindrical fine nozzles (2-250µm) using CNC controlled motion has enabled complex 3D geometries to be fabricated. Additional secondary conductor deposition after firing the ceramic substrate enables the electronic circuitry to be generated without dedicated tooling, masks or templates. This work presents the first fully 3D printed ceramic based electronic substrates. To demonstrate the applications of this printing method a 555 timer circuit with flashing LED has been printed and the components surface mount assembled. The resultant ceramic substrates are dense, mechanically robust and the reflowed circuit functions exactly as intended.

1. Introduction

Across a myriad of industrial sectors, ranging from aviation, space, subsea and energy, high value assets are deployed in harsh environments. These environments are typically defined by challenging high values of temperature, pressure, radiation, vibration and chemically corrosive conditions.

Assets in such conditions present significant challenges in terms of design, operation and maintenance due to limitations in the visibility of the asset within the harsh environment. The ability to monitor these assets is impeded by several issues related to the thermal limits of materials as aggressive ambient conditions may produce sensor drift and failure, power management and communication problems. In such applications, electronics are often exposed to temperatures above 200° C, which exceeds the 150°C limit of traditional Si devices if used without extra cooling mechanisms. However, the trends across these sectors indicate a rapidly growing demand for more sensing and electronics within harsh environments [1-3].

As the demand for electronics capable of withstanding extreme temperature raises, the number of commercially available high temperature wide band gap semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN), is increasing. Currently, SiC is the most mature technology as the fabrication of 300°C integrated circuits and 400°C transistors have been reported already [4, 5]. Such devices have been developed, primarily, to target the needs of the gas & oil sector. However, despite the exceptional advantages of the SiC technology, the lack of reliable packaging materials for high temperatures is a barrier to full exploitation. Poor packaging compromises vital aspects such as heat dissipation, mechanical support and electrical connectivity, consequently reducing performance and lifetime.

As interconnects must tolerate high temperatures and provide high fatigue resistance, soft solders, thermoplastics and epoxies cannot be considered for die mount due to their low melting temperatures. There are a number of alternative options for interconnects for high temperature applications, including Au thermo-compression bonding, silver nanoparticle pastes, Au thick film pastes, and Solid Liquid Interdiffusion (SLID) bonding.

SLID is an interconnection and bonding technique which is based in the rapid formation of an intermetallic compound (IMC) between a high melting point metal and a low melting point metal at a temperature above the melting point of the later. The advantage of the resulting intermetallic compound is that it will have a much higher melting temperature than the processing temperature, therefore allowing subsequent manufacturing steps without the need of decreasing processing temperatures [6]. SLID offers several advantages over the other interconnection systems, e.g. it is faster than thermo-compression bonding [7], joints show higher shear strength than those created using silver nanoparticles paste [8] and it is less complex with a lower processing temperature than Au thick film materials [9, 10]. Examples of SLID bonding are Ag-In, Ag-Sn, Au-In, Au-Sn and Cu-Sn systems.

Cu-Sn system has a processing temperature between 250 °C and 300 °C which forms an intermetallic compound with melting point of 676 °C. Previous results have shown a shear strength of 45 MPa as bonded and resistance around 100 mΩ

[11]. It is well known that the dominant failure mechanism for interconnects is low cycle fatigue caused by a combination of temperature and strain cycling [12]. Previous results by Hoivik *et al.* have shown just slight reduction in the shear strength of Cu-Sn bond pads after being thermally cycled from -40 °C to 150 °C for 1000 cycles over 125 hours [13].

During their lifetime, interconnects used in the aerospace and oil &gas industries are typically exposed concurrently to different loadings such as vibration and thermal shock. However, the contribution of vibration damage to the overall fatigue life of interconnect has not been investigated in any detail previously.Vibration is normally taken as a loading case that only causes elastic material response[14].

With respect to packaging, electronic devices produced from advanced ceramic materials are utilised in a wide range of industries such as automotive, power electronics, aerospace and oil & gas. Ceramic electronic packages have a number of advantages in terms of high reliability, hermetical sealing and ability to withstand high thermal and mechanical shock. However to produce these substrates requires template based manufacturing processes that need large batch production sizes in order to become economically viable. The use of additive manufacturing to generate such products has the potential to revolutionise the production of such devices by enabling: mass customisation, iterative product development, rapid turnaround time of parts, cost effective low-volume production, improved resource efficiency and the generation of more complex structures with increased design freedoms. Micro-extrusion printing methods in which high viscosity ceramic pastes are dispensed through cylindrical fine nozzles (2-250µm) using CNC controlled motion has enabled complex 3D geometries to be fabricated.

In this work we report test vehicles bonded using the Cu-Sn SLID system. In parallel, we also report how micro-extrusion printing methods in which high viscosity ceramic pastes are dispensed through cylindrical fine nozzles (2-250µm) using CNC controlled motion has enabled complex 3D geometries to be fabricated for high temperature electronic packaging applications. Additional secondary conductor deposition after firing the ceramic substrate enables the electronic circuitry to be generated without dedicated tooling, masks or templates. This work presents the first fully 3D printed ceramic based electronic substrates.

The following section outlines the fabrication process of the demonstrator interconnect devices, test procedure and profile, and summary of the characterisation method. Section 3 presents the results and discussion relating to the Cu-Sn interconnects, Section 4 outlines the additive manufacturing process and finally Section 5 presents the primary conclusions of this research.

2. Methodology for Cu-Sn Interconnect Characertisation

A. Demonstrator vehicles preparation

Cu-Sn SLID test vehicles for die shear test were fabricated at the Department of Micro and Nano Systems Technology, at Buskerud and Vestfold University College in Norway.

The vehicles were fabricated by electroplating Cu and Sn on oxidized Si wafers with an Au seed layer. The seed multilayer was formed by a 60 nm TiW adhesion layer, onto which an 800 nm Au film was sputtered. The bond pattern for Cu and Sn electroplating on the Au surface was defined using AZ4562 photoresist. Ar/O_2 (ratio 3:1) plasma treatment was carried out before each electroplating procedure to ensure a clean seed layer surface. The Cu and Sn layers were electroplated using commercially available sulfate-based electrolytes. 4.33 µm of Cu and 0.86 µm were deposited on each wafer using pulse-reverse plating. The bias/reverse current density was set to 10 mA/cm^2, and the bias/reverse pulse was 400 ms/20 ms for both materials.

For the test, bond pads with dimensions of 1.0 mm x 0.8 mm were patterned on each Si wafer. Wafers were bonded using a two step-step temperature profile, on which wafers were heated rapidly at a rate of 7 °C/min and brought in contact at 150 °C, initiating the diffusion process between Cu and Sn early on. This reduces the amount of Sn left in the bond line when reaching the melting temperature of Sn at 231.9 °C, thus reducing the amount of Sn squeezed out. Subsequently, wafers were heated at a rate of 3 °C/min until reaching 260 °C and soaked at least for 10 min, allowing the bond line to be converted to Cu/Cu_3Sn/Cu IMC. At 150 °C, the wafers were brought into contact using a bonding pressure of 20 MPa, which was kept constant throughout the soak time. For more information about the fabrication process refer to [13, 15].

B. System set-up

The testing system consisted of two main units: 1) i.e. the LDS-V650 electrodynamic shaker and 2) a hot plate. A vibration control and data acquisition system was used in order to design and run the vibration test. The hot plate which is fixed on the shaker head, was used as a heat source and also sample fixture. The hot plate was powered and controlled by a temperature controller. Fig. 1 shows the final "shake and bake" system set up.

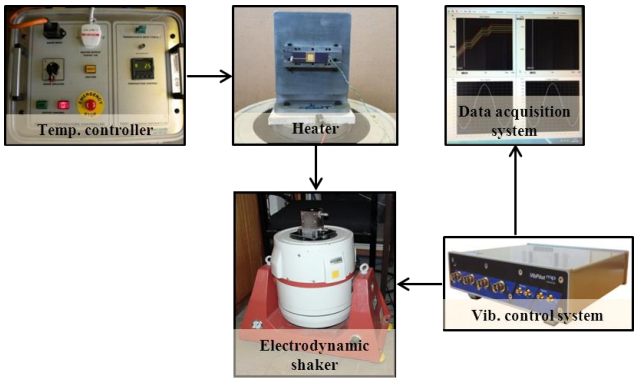

Figure 1 Thermal-Mechanical testing system set up

C. Testing profile

Sets of six Cu-Sn test vehicles were exposed to the standard random vibration test profile, illustrated in Fig. 2 [16], combined with thermal loading at 25 ˚C, 100 ˚C, 200 ˚C and 300 ˚C. The "shake and bake" tests were based on the RTCA/DO-160E Environmental Conditions and Test Procedures for Airborne Equipment standard. Tests were performed in each of the equipment's three orthogonal axes for one-hour-per-axis (total of 3 hours per test). The frequency was ranging from 10Hz to 2000Hz and the acceleration power spectral density (APSD) from 0.02 G^2/Hz to 0.08 G^2/Hz. The APSD levels that correspond to each test curve frequency break point can be found in Table 1 [16].

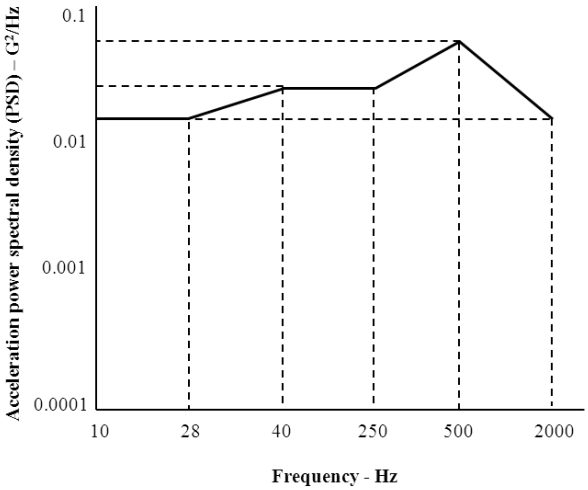

Figure 2 Standard random vibration test curve for equipment installed in fixed-wing aircraft with turbofan engines

Table 1 Acceleration power spectral density levels corresponding to each test curve frequency break point

Test levels at test curve frequency break points						
Frequency (Hz)	10	28	40	250	500	2000
APSD (G^2/Hz)	0.02	0.02	0.04	0.04	0.08	0.02

1) Analysis technique: Shear testing was performed to characterize the mechanical strenght of the bond pads after the "shake and bake" test. In order to calculate the efective shear strenght the bonded area must be known. Some of the samples were cross sectioned to be analysed by optical microscopy or scanning electron microscopy (SEM).

D. Shear testing

The die shear tests were performed using a Dage Series 4000 Bondtester with a 100 kg load cartridge. The shear tool height was set at 56.0 µm above the surface of the substrate and shear speed of 70.0 µm/s. Die shear test was performed on four of the six samples from each set with the remaining two samples used for the cross-sectional analysis.

E. Cross sectional analysis

After tests, 2 samples from each set were diced using a 300µm thick fully sintered diamond blade rotating at 13,000 RPM. As a first approach the cross-sectioned samples were inspected, without polishing, using a Leica DM6000 M microscope with an N Plan L 100X/0.75 BD objective.

3. Results and Discussion

F. Shear testing

Fig. 3 shows the average die shear strength for sets of 4 samples exposed to the vibration/thermal loading described in Sec. II-C and Fig. 4 shows samples exposed only to thermal loading without the vibration shock.

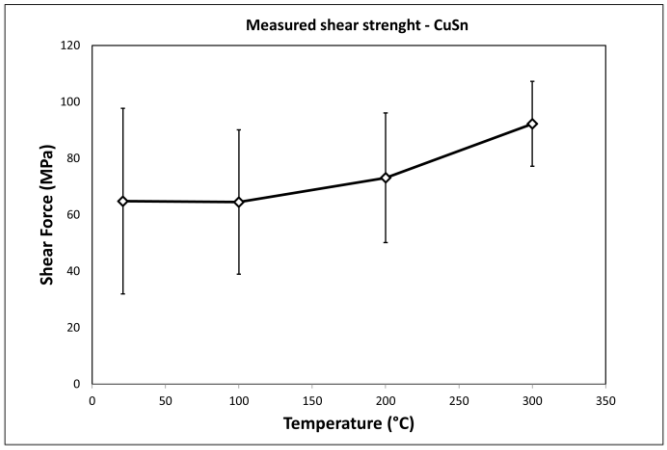

Figure 3 Measured shear strength for sets of samples exposed concurrently to vibration/thermal loading

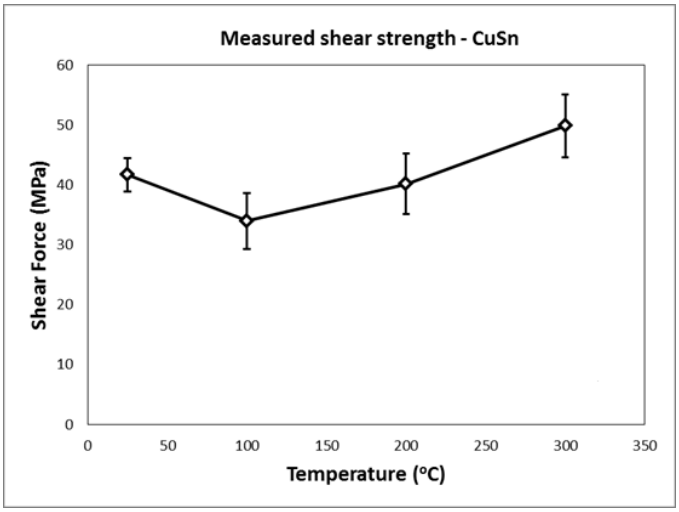

Figure 4 Measured shear strength for sets of samples exposed only to thermal loading

As indicated within Fig 3&4 the samples exposed to thermomechanical effects have an increase in die shear force, with the 300 °C samples exhibiting an increase of 40 MPa. Both sets of samples exhibit an increase in die shear strength beyond 100 °C. At 300 °C there is a compositional change with increasing alloy presence as the Cu layers are incorporated into the CuSn alloy.

G. Microstructural analysis

As mentioned previously, as I first approach, cross-sectioned samples were inspected without being polished. The next group of images show the cross-section of samples exposed to vibration and thermal loading of 21 °C, 100 °C, 200 °C and 300 °C, respectively.

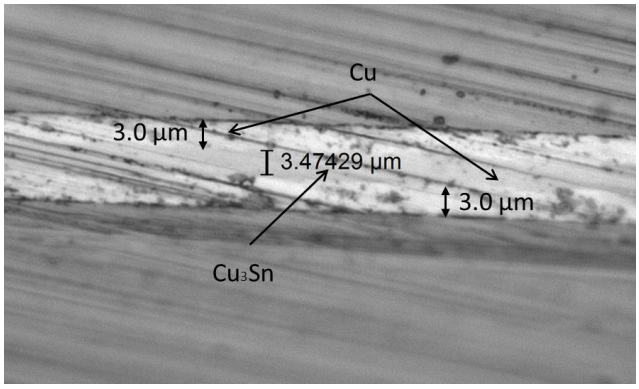

Figure 5 Cross-section of sample exposed to vibration @21°C

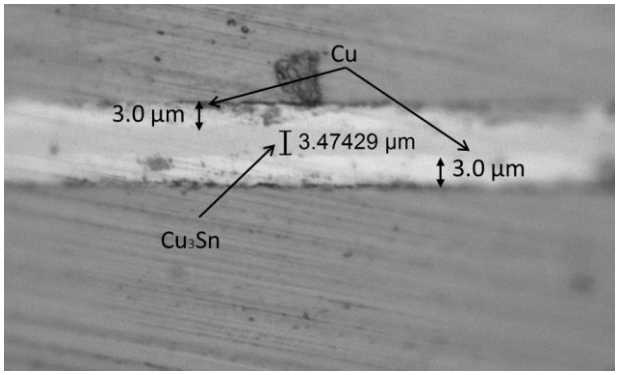

Figure 6 Cross-section of sample exposed to vibration @100 °C

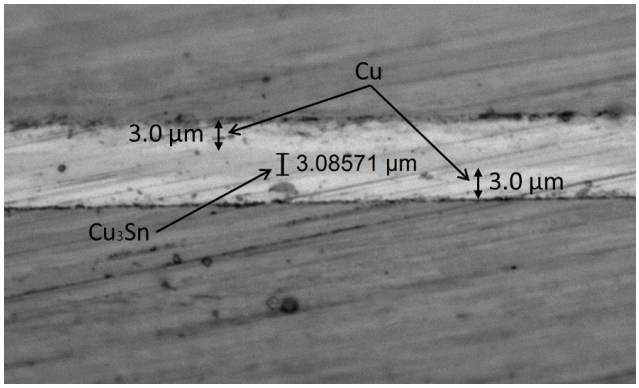

Figure 7 Cross-section of sample exposed to vibration @200°C

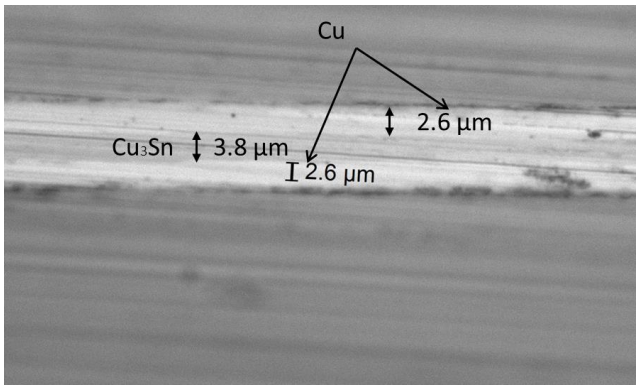

Figure 8 Cross-section of sample exposed to vibration @300 °C

The optical microscopy images indicate that there is a gradual increased in the alloy composition within the interconnect structure. It would appear that increasing alloy composition produces a desirable increase in shear strength.

4. Additive Manufacturing of Ceramic Packaging

A 5-axis table is used to drive the dispensing head with motion accuracy ±25µm, shown in Fig. 8. The dispensing head equipped with a piezoelectric actuator is used for printing of a small particle size distribution alumina based paste supplied by Morgan Advanced Materials which exhibited the required viscoelastic characteristics to enable printing successfully down through 150µm nozzles. The printing process begins by extruding a perimeter defining the layer features. The layer is then in-filled using a rectilinear infill pattern. The process is then repeated layer-by-layer to build up the substrate. In this case 4 layers have been printed. The green part is then fired at 1600°C and shrinkages around 15% from the process.

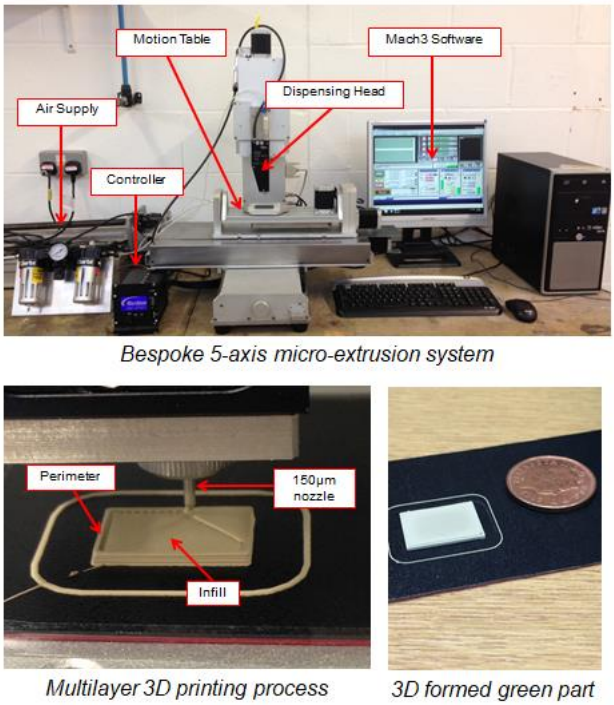

Figure 8 5 axis micro-extrusion system, image of the 3D printing process.

Cross sectioning of the substrate reveals a high density fired part with the printed layers not visible, shown in Fig. 9. However polishing of the cross-sectioned samples needs to be improved as grains have been cleaved from the sample surface. Also, elimination of air entrapment in the paste prior to printing is required.

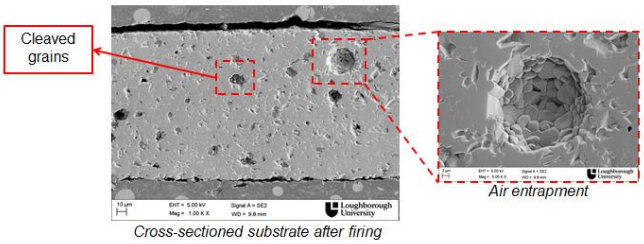

Figure 9 Cross-section of the ceramic microstructure

The Ag filled LTCC paste was selectively deposited onto the fired ceramic substrate. To test the feasibility of this process a surface mount 555 timer circuit with flashing LED, timer chip and discrete components was designed. The circuit was deposited using a 200µm nozzle. After printing the substrate was fired again using a profile of 3°C/min to 100°C, 2°C/min to 450°C, 10°C/min to 865°C and hold for 20 minutes. The final line width after firing was approximately 700µm. Using a smaller nozzle diameter in addition to adjustments to the rheological properties of the paste material and a reduction of particle size could enable a smaller nozzle diameter and resulting finer track widths.

The fired conductor lines exhibited a strong adhesion to the ceramic substrate and a low resistance similar to conventional LTCC conductive tracks. The ceramic substrate was processed using a conventional surface mount assembly process of solder paste deposition, pick and place of the individual components followed by a reflow process in a convection oven. The 555 timer circuit consists of three capacitors, one LED, four resistors, one transistor and one 555 timer, shown in Fig. 10. The solder paste was dispensed rather than using a stencil template in order to prove this whole process could be digitally driven thereby enabling mass customised production of parts and also rapid iterative product development.

The first board assembled and reflowed worked exactly as intended thereby proving the feasibility of this approach. This work demonstrates the world's first fully 3D printed ceramic electronic substrate completely compatible with conventional surface mount packaging.

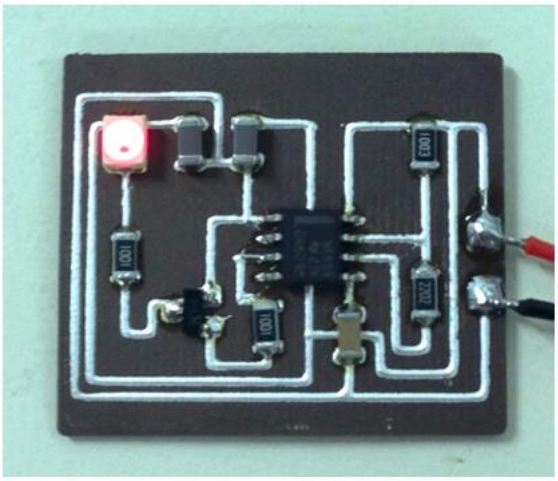

Figure 10 Fully functioning 555 timer circuit

5. Conclusions

Within this research we have fabricated, characterized and analyzed CuSn interconnects for harsh environment applications. The suitability of this interconnect technology has been validated through the seminal testing with a custom shake & bake system. The compositional changes with temperature appear to influence the die shear strength of the samples. Interestingly the influence of the vibrational forces has further enhanced this property. Further testing is required to validate the influence of the compositional change on the electrical properties of the interconnects, as well as a detailed analysis of the resultant grain properties. However, these preliminary results indicate a potential design freedom in the optimization of the interconnects with respect to structural integrity and electrical properties for harsh environments.

The customised Additive Manufacturing process represents the first 3D printed ceramic based electronic substrates. The resultant ceramic substrates are dense, mechanically robust and the reflowed circuit functions exactly as intended.

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